REMARKS

Claims 1-13 and 15-19 are now pending in this application for which applicants seek reconsideration.

Amendment

Independent claims 1 and 4-7 have been amended to define that each of the delay circuits controls the delay setting for each of the speaker units. New dependent claims 15-19 correspond to the claims granted in the counterpart Japanese application. See Fig. 4, for example, for support. No new matter has been introduced.

Art Rejection

Claims 1, 4, and 6 were rejected under 35 U.S.C. § 102(e) as anticipated by Yoshino (USP 7,054,448). Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) as unpatentable over Yoshino in view of Yeap (USP 4,118,601). Claim 5 was rejected under § 103(a) as unpatenable over Yeap in view of Grimani (USP 6,498,852). Lastly, claims 7-13 were rejected under § 103(a) as unpatentable over Yoshino in view of Aylward (USP 6,240,189).

In maintaining the art rejections, the examiner alleges that the claimed directivity control (using a delay setting for each of the delay circuits based on the desired focal position of a sound wave beam to be directed to and the position of each of the speaker units) is known, relying on Yoshino. Applicants disagree for the following reasons.

First, Yoshino does not disclose an array speaker unit, but rather a conventional speaker setup as illustrated in Fig. 6. **Each speaker receives a discrete dedicated signal from one of SPFL, SPFR, SPC, SPRL, SPRR, SPWF, SPSBL, and SPSBR**. In contrast, the claimed invention does not have a single discrete channel output to a single speaker. Rather, all channels are output to all of the array of speakers. Using delays, the directivity of a sound beam created by the array speakers is controlled.

Second, the examiner alleges that Yoshino discloses the claimed delay circuit configuration. In Yoshino, each speaker has an associated dedicated delay circuit. In contrast, the claimed invention calls for providing a delay circuit for each sound signal (e.g., channel), which is output to all the speakers. For added clarity, of the independent claims define that each of the delay circuit controls the delay setting for each of the speaker units. For example, referring to Figs. 2, 6, etc., of the present disclosure, each of the delay circuits 1 and 3 for channels 0, 1 outputs to all the speakers 7-1 to 7-n instead to only a single dedicated speaker.

As the claims positively define a directivity control circuit in an array speaker unit in which each of the delay circuit controls the delay setting for all of the speaker units, applicants submit that the pending claims clearly define over the applied references.

Conclusion

Applicants submit that the pending claims are in condition for allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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DATE

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